PVP 14

Code: CS2T4

I B.Tech - II Semester – Regular/Supplementary Examinations
April - 2018

DIGITAL LOGIC DESIGN
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Convert 12.95 decimal number to its binary equivalent.
b) Convert $(615)_8$ to its hexadecimal number.
c) Define gray code and write gray codes for 0 to 9 decimal numbers.
d) Explain Demorgan's theorems.
e) Define how XOR and XNOR gates act as Inverter?
f) Define decoder.
g) Define half adder.
h) What is PLA? How it differs from PROM?
i) Write the difference between PROM, PLA and PAL.
j) What is race around condition?
k) What is the difference between combinational circuits and sequential circuits?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Perform the subtraction using 9's complement method for 592.6-887.9 8 M

   b) Assume that the even parity hamming code in example 0110011 is transmitted and that 0100011 is received. The receiver does not know what was transmitted. Determine bit location where error has occurred using received code? 8 M

3. a) Convert the given expression in standard SOP form.
   f(A,B,C)=A+AB+B'C 4 M

   b) Reduce the following function using k-map technique. 12 M

   i) $f(A,B,C,D) = \Sigma\, m(5,6,7,12,13)+ \Sigma d(4,9,14,15)$

   ii) $f(P,Q,R,S)= \Pi M(0,3,4,7,8,10,12,14)+d(2,6)$

4. a) Design a 4-bit parallel adder using full adders. 8 M

   b) Design 5-to-32 decoder using one 2-to-4 decoder and four 3-to-8 decoder ICs. 8 M

5. a) Illustrate how a PLA can be used for combinational logic design with reference to following functions:

i) $f_1(A,B,C)= \Sigma\, m(0,1,3,4)$

ii) $f_2(A,B,C)= \Sigma\, m(1,2,3,4,5)$.

Realize the same assuming that a PLA is available. 10 M

b) Design a combinational circuit using a PROM. The circuit accepts 3-bit binary number and generate its equivalent Excess-3 code. 6 M

6. a) Derive the characteristic equation of JK flip-flop from Excitation table. 8 M

b) Design a MOD-5 synchronous counter using JK flip-flops and implement it. Also construct a timing diagram. 8 M